

ATTORNEY DOCKET NO.
080086.0163 (formerly 062986.0296)
(824.51)

PATENT APPLICATION
10/696,146

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Michael B. Galles, et al.
Serial No.: 10/696,146
Filing Date: October 29, 2003
Confirmation No.: 5506
Group Art Unit: 2181
Examiner: William M. Treat
Title: MULTI-PURPOSE PROCESSOR SYSTEM AND
METHOD OF ACCESSING DATA THEREIN

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

APPEAL BRIEF

Applicant has appealed to the Board of Patent Appeals and Interferences from the final decision of the Examiner mailed April 29, 2009 finally rejecting Claims 1-20. Applicant respectfully submits herewith their brief on appeal.

REAL PARTY IN INTEREST

The present Application was assigned by the inventors to Silicon Graphics, Inc., a Delaware corporation, as indicated by an assignment from the inventors for the parent application recorded on October 15, 1999 in the Assignment Records of the United States Patent and Trademark Office at Reel 010325, Frames 0832-0836. Silicon Graphics, Inc. assigned a security interest in the Application to Wells Fargo Foothill Capital, Inc., as evidence by a document recorded on August 19, 2005 in the Assignment Records of the United States Patent and Trademark Office at Reel 016871, Frames 0809-0840. Silicon Graphics, Inc. also assigned a security interest in the Application to General Electric Capital Corporation, as evidence by a document recorded on August 24, 2006 in the Assignment Records of the United States Patent and Trademark Office at Reel 018545, Frames 0777-0841.

RELATED APPEALS AND INTERFERENCES

There are no known appeals or interferences that will directly affect or be directly affected by or have a bearing on the Board's decision in this pending appeal.

STATUS OF CLAIMS

Claims 1-20 stand rejected pursuant to a Final Action mailed April 29, 2009. Claims 1-20 are all presented for appeal.

STATUS OF AMENDMENTS

A Response to Examiner's Final Action was filed on May 19, 2005 in response to a Final Action mailed March 23, 2005. Claims 1, 11, and 16 were amended. A Request for Continued Examination was filed on June 23, 2005 in response to an Advisory Action mailed June 3, 2005 in order to have the Response to Examiner's Final Action of May 15, 2005 entered and considered by the Examiner. A Response to Examiner's Action was filed on December 8, 2005 in response to an Official Action mailed September 9, 2005. No further amendments were made to the claims. A Response to Examiner's Final Action was filed on April 24, 2006 in response to a Final Action mailed February 23, 2006. No further amendments were made to the claims. A Request for Continued Examination was filed on May 23, 2006 in response to an Advisory Action mailed June May 9, 2006 in order to provide amendments to the specification. No further amendments were made to the claims. A Response to Examiner's Final Action was filed on October 6, 2006 in response to a Final Action mailed August 9, 2006 providing another amendment to the specification. No further amendments were made to the claims. Applicant filed a Notice of Appeal and Request for Pre-Appeal Brief Review on November 9, 2006 in Response to an Advisory Action mailed October 19, 2006. A Notice of Panel Decision from Pre-Appeal Brief Review issued on December 21, 2006 stating that the appeal is to proceed to the Board of Patent Appeals and Interferences. Prosecution was reopened and an Office Action was issued April 24, 2008. A Response to Examiner's Action was filed on July 24, 2009 in response thereto. No further amendments were made to the claims. A Response to Examiner's Action was filed on February 3, 2009 in response to another Office Action issued November 3, 2009. Claims 1, 4, 11, 15, and 16 were amended.

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Applicant filed a Notice of Appeal on August 31, 2009 in
Response to a Final Action issued April 29, 2009.

SUMMARY OF CLAIMED SUBJECT MATTER

With respect to Independent Claim 1, a multi-processor system 10 is provided. (See FIGURE 1 and page 7, lines 2-3). The multiprocessor system 10 includes a plurality of processors 12. (See FIGURE 1 and page 7, lines 3-4). Each processor 12 includes an integrated memory 16 operable to provide/receive/store data. (See FIGURE 1 and page 7, lines 5-8). Each processor includes a central processing unit 20 having an integrated memory controller 30 operable to control access to the integrated memory 16 and an integrated memory directory 18 operable to maintain a plurality of memory references to data within the integrated memory 16. (See FIGURES 1 and 2 and page 8, lines 24-27 as amended). The multiprocessor system 10 includes an external switch 14 coupled to each of the plurality of processors 12. (See FIGURE 1 and page 7, lines 3-10). The external switch 14 is operable to pass data to and from any of the plurality of processors 12. (See FIGURE 1 and page 7, lines 8-10). The external switch 14 includes an external directory 22. (See FIGURE 1 and page 7, lines 7-8). The external directory 22 is operable to provide a memory reference for each of the plurality of processors 12 to remote data that is not provided within its own integrated memory directory 18. (See FIGURE 1 and page 7, line 28, to page 8, line 5).

With respect to Independent Claim 11, a method of accessing data in a multi-processor system 10 is provided. The method includes storing information in a local memory 16 where the local memory is integrated within a particular one of a plurality of processors 12 of the multi-processor system 10. (See page 7, lines 5-7). A list of memory references to the information in the local memory 16 is maintained in a memory directory 18 integrated with a central processing unit

20 of the particular one of the plurality of processors 12. (See FIGURES 1 and 2; page 7, lines 5-7 and 14-16; and page 8, lines 24-27 as amended). A request for data is generated. (See page 7, lines 28, to page 8, line 2). A determination is made as to whether the data is associated with information stored in the local memory 16 and has a memory reference in the memory directory 18. (See page 7, lines 28-31). The request is forwarded to an external switch 14 in response to the data not having a memory reference in the memory directory 18. (See page 7, line 28, to page 8, line 1). Data not having a memory reference to the local memory 16 in the memory directory 18 is stored in a remote memory 16. (See page 7, lines 28-31). A memory reference for the data is identified in response to the request. (See page 8, lines 3-5). The data from the remote memory 16 is obtained via the external switch 14 in response to the identified memory reference. (See page 8, lines 3-5).

With respect to Independent Claim 16, a processor 12 in a multi-processor system 10 is provided. (See FIGURE 1 and page 7, lines 2-3). The processor 12 includes a local memory 16 integrated in the processor 12 and operable to provide/receive/store data. (See FIGURE 1 and page 7, lines 5-7). The processor 12 includes a central processing unit 20. (See FIGURES 1 and 2 and page 7, lines 5-7). A memory controller 30 is integrated in the central processing unit 20 and operable to control access to and from the local memory 16. (See FIGURES 1 and 2 and page 8, lines 24-32 as amended). A memory directory 18 is integrated in the central processing unit 20 and operable to maintain memory references to data within the local memory 16. (See FIGURES 1 and 2 and page 7, lines 5-7 and 14-16). The memory directory 18 is operable to generate a data request for data not having a memory reference

in the memory directory 18. (See Page 7, line 28, to page 8, line 1). The processor 12 includes a network interface 32 integrated in the processor 12 and operable to provide the data request to an external directory 22 external to the processor 12. (See FIGURE 2 and page 8, lines 27-29). The network interface 32 is operable to receive the data according to the data request. (See FIGURE 2 and page 8, lines 27-29).

GROUND OF REJECTION TO BE REVIEWED ON APPEAL

1. Claims 1-10 and 16-20 stand rejected under 35 U.S.C. §112, first paragraph, for containing subject matter not described in the specification.

2. Claims 1-10 and 16-20 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite.

3. Claims 1, 2, and 4-20 stand rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,890,217 issued to Kabemoto, et al.

4. Claims 1, 2, 5, 6, 9-11, and 13-17 stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 5,944,780 issued to Chase, et al.

5. Claims 3, 10, 18, and 20 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,944,780 issued to Chase, et al.

6. Claim 3 stands rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,890,217 issued to Chase, et al.

7. Amendments made to the specification stand objected to under 35 U.S.C. §132(a) as introducing new matter.

8. The drawings stand objected under 37 C.F.R. §1.84(p)(5) for not including reference signs mentioned in the specification.

9. The drawings stand objected under 37 C.F.R. §1.84(p)(5) for including reference signs not mentioned in the specification.

10. Claims 1-20 stand rejected under 35 U.S.C. §103(a) as being unpatentable over "The SGI Origin: A ccNUMA Highly Scalable Server" published by Laudon, et al. in view of "The MIPS Superscalar Microprocessor" published by Yeager in view of "An Evaluation of Directory Schemes for Cache Coherence"

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published by Agarwal, et al. and further in view of "Origin
2000 ccNUMA Architecture" published by Goyette.

ARGUMENT

1. Claims 1-10 and 16-20 stand rejected under 35 U.S.C. §112, first paragraph, for containing subject matter not described in the specification.

For the written description requirement, the specification must reasonably convey to those skilled in the art that applicant was in possession of the claimed invention as of the date of the invention. M.P.E.P. §2106(V)(B).

The claimed invention subject matter need not be described literally, i.e., using the same terms, in order for the disclosure to satisfy the description requirement. M.P.E.P. §2106(V)(B). Support for the central processing unit having an integrated memory controller as required in Independent Claims 1 and 16 is clearly provided in FIGURE 2. FIGURE 2 is a detailed view of central processing unit 20. This is supported by the fact that the element is labeled with reference numeral 20 and includes directory 18 consistent with what is shown in FIGURE 1. Moreover, a link to memory 16, and not memory 16 itself, is shown in FIGURE 2 providing further basis that FIGURE 2 is a detailed view of CPU 20 within processor 12. Accordingly, memory controller 30 and memory directory 18 are clearly shown to be within central processing unit 20. Applicant's specification at page 7, lines 5-7, particularly discloses that these components are integrated with memory 16 into a single device, processor 12. Thus, the specification provides clear support for the claim language. Dependent Claims 2-10 and 17-20 respectively depend from Independent Claims 1 and 16 and are also in accordance with 35 U.S.C. §112, first paragraph, for the reasons specified above. Therefore, Applicant respectfully submits that Claims 1-10 and 16-20 are in accordance with 35 U.S.C. §112, first paragraph.

2. Claims 1-10 and 16-20 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite.

As pointed out above, FIGURE 2 and Applicant's specification provide ample support for the claimed invention. FIGURE 2 clearly shows a central processor 20 having a memory controller 30 and a memory directory 18 integrated, along with memory 16, into the single device of processor 12 as provided in Independent Claims 1 and 16. Moreover, the term 'integrated' is clearly defined in the specification as being within a single device. Dependent Claims 2-10 and 17-20 respectively depend from Independent Claims 1 and 16 and are also in accordance with 35 U.S.C. §112, second paragraph, for the reasons specified above. Therefore, Applicant respectfully submits that Claims 1-10 and 16-20 are in accordance with 35 U.S.C. §112, second paragraph.

3. Claims 1, 2, and 4-20 stand rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,890,217 issued to Kabemoto, et al.

To anticipate a claim under 35 U.S.C. §102(e), a single prior art reference must teach each and every limitation as set forth in the claims. Since the cited prior art reference does not teach each and every element set forth in the claims, Applicant respectfully traverses this rejection.

Independent Claim 1 recites ". . . each processor including an integrated memory operable to provide/receive/store data, each processor including a central processing unit with an integrated memory controller operable to control access to the integrated memory and an integrated memory directory operable to maintain a plurality of memory references to data within the integrated memory" Similarly, Independent Claim 16 recites ". . . a local memory integrated in the processor and operable to provide/receive/store data; a central processing unit; a memory controller integrated in the central processing unit and operable to control access to and from the local memory; a memory directory integrated in the central processing unit and operable to maintain memory references to data within the local memory, the memory directory operable to generate a data request for data not having a memory reference in the memory directory" Independent Claim 11 recites ". . . storing information in a local memory, the local memory being integrated within a particular one of a plurality of processors of the multi-processor system; maintaining a list of memory references to the information in the local memory in a memory directory integrated with a central processing unit of the particular one of the plurality of processors"

By contrast, the Kabemoto, et al. patent shows processor and cache units separate from each other and a separate memory control module. Moreover, a directory memory is disclosed as being separate and apart from the processor. The Examiner seems to refer to processor element 14-1 of the Kabemoto, et al. patent in stating that each component of the claimed invention is found therein but has not shown how the processor 16-1 itself includes each component of the processor and central processing unit of the claimed invention. The processor element 14-1 of the Kabemoto, et al. patent includes a processor 16-1, a cache unit 18-1, and a snoop unit 20-1. The Examiner shows that the processor 16-1 of the Kabemoto, et al. patent includes a memory 36 and 38 but readily admits that a memory controller 35 and a memory directory 40 of the Kabemoto, et al. patent are not included in its processor 16-1 by showing that the memory controller 35 and the memory directory 40 are in the cache unit 18-1 which is separate and apart from the processor 16-1. As a result, the processor of the Kabemoto, et al. patent does not include the resources and functionality of the processor and central processing unit in the claimed invention. Thus, the Kabemoto, et al. patent does not have a processor that includes an integrated memory as required by Independent Claims 1, 11, and 16 and a central processing unit with an integrated memory controller as required by Independent Claims 1 and 16 and an integrated memory directory as required by Independent Claims 1, 11, and 16. Dependent Claims 2, 4-10, 12-15, and 17-20 depend respectively from Independent Claims 1, 11, and 16 and are patentably distinct from the Kabemoto, et al. patent for the reasons discussed above. Therefore, Applicant respectfully submits that Claims 1, 2, and 4-20 are not anticipated by the Kabemoto, et al. patent.

Applicant has consistently shown how the Kabemoto, et al. patent fails to support a rejection of the claims. However, the Examiner continued to provide an improper omnibus rejection of the claims in contradiction to M.P.E.P. §707.07(d), making it difficult to understand the Examiner's position. The Examiner merely directed Applicant to specific portions of the Kabemoto, et al. patent but failed to show how the specific portions of the Kabemoto, et al. patent met the terms of the claims. Applicant has read the specific portions of the Kabemoto, et al. patent identified by the Examiner but respectfully submits that these cited portions fail to disclose each and every one of the elements of the claimed invention. Applicant respectfully requested the Examiner to provide a complete and proper analysis of the claims by showing how each and every limitation of each and every claim is possibly met by the Kabemoto, et al. patent.

4. Claims 1, 2, 5, 6, 9-11, and 13-17 stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 5,944,780 issued to Chase, et al.

To anticipate a claim under 35 U.S.C. §102(e), a single prior art reference must teach each and every limitation as set forth in the claims. Since the cited prior art reference does not teach each and every element set forth in the claims, Applicant respectfully traverses this rejection.

Independent Claim 1 recites ". . . each processor including an integrated memory operable to provide/receive/store data, each processor including a central processing unit with an integrated memory controller operable to control access to the integrated memory and an integrated memory directory operable to maintain a plurality of memory references to data within the integrated memory" Similarly, Independent Claim 16 recites ". . . a local memory integrated in the processor and operable to provide/receive/store data; a central processing unit; a memory controller integrated in the central processing unit and operable to control access to and from the local memory; a memory directory integrated in the central processing unit and operable to maintain memory references to data within the local memory, the memory directory operable to generate a data request for data not having a memory reference in the memory directory" Independent Claim 11 recites ". . . storing information in a local memory, the local memory being integrated within a particular one of a plurality of processors of the multi-processor system; maintaining a list of memory references to the information in the local memory in a memory directory integrated with a central processing unit of the particular one of the plurality of processors"

By contrast, the station 12 of the Chase, et al. patent equated by the Examiner as the claimed processor shows a processor 18 and a storage 21 with a cache 20 separate and apart from its processor 18. Thus, the storage 21 and cache 20 of the Chase, et al. patent are not integrated within its processor 18 as would be required by the claimed invention. Therefore, the Examiner has failed to show how the Chase, et al. patent has a processor with an integrated memory as required in Independent Claims 1, 11, and 16 when the Chase, et al. patent specifically shows a separate processor 18 and a separate storage 20 that is not included within the processor 18.

The Chase, et al. patent expressly discloses a cache directory 16 in a directory server 17 that is separate and apart from station 12 and its processor 18 and storage 21. The Chase, et al. patent clearly discloses the use of a cache directory 16 in a server 17 separate and remote from any of its stations 12 for use with cache 20 within station 12. The Chase, et al. patent clearly teaches away from any use of a directory within its station 12 and being integrated with its processor 18 let alone being integrated within a central processing unit as required by the claimed invention. Thus, the memory directory of the Chase, et al, patent is not integrated in a central processing unit of a processor as required by Independent Claims 1, 11, and 16. In fact, the memory directory 16 is disclosed in the Chase, et al. patent as also being separate from a processor 18 within its directory server 17.

Further, the Chase, et al. patent provides no mention of a memory controller within station 12 or processor 18 let alone any integration of a memory controller within its processor 18 as required in Independent Claims 1 and 16. All

of the portions of the Chase, et al. patent cited by the Examiner clearly show a memory controller being separate and apart from its corresponding processor. Thus, not only does the Chase, et al. patent fail to show a local memory integrated within a processor and a memory controller integrated within a central processing unit of a processor, there is also no support in the Chase, et al. patent for a memory directory also integrated in the central processing unit as required by the claimed invention.

Applicant's specification specifically shows that the term 'integrated' defines these elements as being within a single device, the processor. Thus, contrary to the Examiner's assertion, Applicant's specification clearly limits the claimed elements to a single device through the use of the word 'integrated' provided in the claims. The Chase, et al. patent teaches away from this integration by having all of the claimed elements in separate devices. The processor of the Chase, et al. patent does not include the resources and functionality of the processor or the central processing unit in the claimed invention. As a result, the Examiner has not provided any teaching within the Chase, et al. patent to support the rejection of the claims. Thus, without a reference that discloses each and every limitation or a reference combinable with the Chase, et al. patent to support a rejection, the Chase, et al. patent by itself is insufficient to support a rejection of the claimed invention. Dependent Claims 5 and 7-10 depend from Independent Claim 1 and are patentably distinct from the Chase, et al. patent for the reasons discussed above. Therefore, Applicant respectfully submits that Claims 1, 5, and 7-10 are not anticipated by the Chase, et al. patent.

Applicant has consistently shown how the Chase, et al. patent fails to support a rejection of the claims. However, the Examiner continued to provide an improper omnibus rejection of the claims in contradiction to M.P.E.P. §707.07(d), making it difficult to understand the Examiner's position. The Examiner merely directed Applicant to specific portions of the Chase, et al. patent but failed to show how the specific portions of the Chase, et al. patent met the terms of the claims. Applicant has read the specific portions of the Chase, et al. patent identified by the Examiner but respectfully submits that these cited portions fail to disclose each and every one of the elements of the claimed invention. Applicant respectfully requested the Examiner to provide a complete and proper analysis of the claims by showing how each and every limitation of each and every claim is possibly met by the Chase, et al. patent.

5. Claims 3, 10, 18, and 20 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,944,780 issued to Chase, et al.

Independent Claim 1, from which Claims 3 and 10 depend, and Independent Claim 16, from which Claims 18 and 20 depend, have been shown above to be patentably distinct from the Chase, et al. patent. Therefore, Applicant respectfully submits that Claims 3, 10, 18, and 20 are patentably distinct from the Chase, et al. patent.

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6. Claim 3 stands rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,890,217 issued to Kabemoto, et al.

Independent Claim 1, from which Claim 3 depends, has been shown above to be patentably distinct from the Kabemoto, et al. patent. Therefore, Applicant respectfully submits that Claim 3 is patentably distinct from the Kabemoto, et al. patent.

7. Amendments made to the specification stand objected to under 35 U.S.C. §132(a) as introducing new matter.

Applicant respectfully submits that no new matter has been added into the specification. Changes to the specification have been made to provide consistency with what is clearly shown in FIGURE 2 and requested by the Examiner. Attached herewith is a copy of a page from the Request for Continued Examination of May 23, 2009 showing the minor changes to the specification in order to provide consistency with the drawings as requested by the Examiner. Also attached herewith is a copy of the drawings of which no amendments were made. FIGURE 2 clearly illustrates the make up of central processing unit 20 of processor 12. The element is labeled 20 as similarly provided in FIGURE 1. Memory directory 18 is consistently shown to be within element 20, the central processing unit, in both FIGURES 1 and 2. Furthermore, the absence of memory 16 from FIGURE 2 is further consistent with FIGURE 2 being only a depiction of central processing unit 20. Thus, changes to the specification have been appropriately made based on what is shown in FIGURE 2 without adding any new matter. Therefore, Applicant respectfully submits that the changes made to the specification are in accordance with 35 U.S.C. §132(a).

8. The drawings stand objected under 37 C.F.R. §1.84(p)(5) for not including reference signs mentioned in the specification.

The Examiner has not indicated which reference numerals are missing from the drawings. FIGURE 2, in conjunction with FIGURE 1, includes the appropriate reference signs mentioned in Applicant's specification. Therefore, Applicant respectfully submits that the drawings are in accordance with 37 C.F.R. §1.84(p)(5).

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9. The drawings stand objected under 37 C.F.R. §1.84(p)(5) for including reference signs not mentioned in the specification.

Applicant's specification has been amended to be consistent with FIGURE 2 to include a description of reference numeral 20 as requested by the Examiner. Therefore, Applicant respectfully submits that the drawings are in accordance with 37 C.F.R. §1.84(p)(5).

10. Claims 1-20 stand rejected under 35 U.S.C. §103(a) as being unpatentable over "The SGI Origin: A ccNUMA Highly Scalable Server" published by Laudon, et al. in view of "The MIPS Superscalar Microprocessor" published by Yeager in view of "An Evaluation of Directory Schemes for Cache Coherence" published by Agarwal, et al. and further in view of "Origin 2000 ccNUMA Architecture" published by Goyette.

Independent Claims 1, 11, and 16 recite in general a processor including an integrated memory operable to provide/receive/store data, each processor including a central processing unit with an integrated memory controller operable to control access to the integrated memory and an integrated memory directory operable to maintain a plurality of memory references to data within the integrated memory and at least one memory reference to data within an integrated memory of a different processor. The Examiner indicates that the Laudon, et al. publication discloses the use of a R10000 processor and the Yeager publication discloses that the R10000 processor includes secondary caches and a CPU where the CPU has an internal memory controller to control access to the secondary caches. Contrary to the Examiner's assertion, the Yeager publication fails to disclose that the R10000 CPU includes an integrated memory directory as required by the claimed invention. As shown in Figure 1, the Yeager publication clearly shows a directory separate from its CPU units. Moreover, there is no disclosure in the Yeager publication that the directory maintains memory references to data in its secondary caches.

The Examiner asserts that anyone of ordinary skill would know how to include the Mem & Dir onto the Hub Chip of the Laudon, et al. publication based on advances in fabrication in order to reduce time in propagating signals and provide

savings in power. However, the Examiner fails to provide any support for such a conclusory statement. The Examiner has failed to provide any proof for such an assertion. In addition, there has been no showing that signal propagation delay and power are real problems contemplated in the prior art that would lead to the features of the claimed invention. Moreover, the Examiner has failed to show that such knowledge was available at the time of the present invention. In addition, the Examiner equates the Translation Look-aside Buffer of the Yeager publication as an integrated memory directory. However, the Translation Look-aside Buffer of the Yeager publication merely translates virtual addresses to physical addresses and fails to disclose any ability to maintain a memory reference to data stored in an integrated memory of a different processor as required by the claimed invention. Support for the above recitation can be found at page 7, lines 14-20, of Applicant's specification.

Independent Claim 11 recites ". . . maintaining a list of memory references to the information in the local memory in a memory directory integrated with a central processing unit of the particular one of the plurality of processors; generating a request for data; determining whether the data is associated with information stored in the local memory and has a memory reference in the memory directory; forwarding the request to an external switch in response to the data not having a memory reference in the memory directory, wherein the data not having a memory reference to the local memory in the memory directory is stored in a remote memory . . ." By contrast, the Examiner merely rejects Claim 11 as failing to define over rejected Claims 1-10. However, Claim 11 does define over Claim 1 by being directed to an operation including steps not provided in Claim 1. Thus, the Examiner has failed to show that either of

the Laudon, et al. or Yeager publications disclose the operation provided by Claim 11.

Independent Claim 16 recites ". . . a memory directory integrated in the central processing unit and operable to maintain memory references to data within the local memory, the memory directory operable to generate a data request for data not having a memory reference in the memory directory . . ." By contrast, as pointed out above with reference to Claim 1, the Yeager publication fails to disclose a memory directory integrated in its CPU and operable to maintain memory references to data in the local memory of the processor and to maintain at least one memory reference to data in an integrated memory of a different processor. Moreover, the Yeager publication fails to disclose any directory operable to generate a data request for data not having a memory reference in the directory as required by the claimed invention.

The Agarwal publication is merely recited for disclosing that directory schemes were known in the art prior to the invention of the present Application. However, the Agarwal publication fails to remedy the deficiencies in the Laudon, et al. and Yeager publications as discussed above. The Examiner further recites the Goyette publication for its disclosure that a ccNUMA system predates the invention of the present Application. However, the Examiner has failed to show that the features of the claimed invention were a part of any ccNUMA system prior to the earliest effective filing date of the present Application. In fact, the Goyette publication discloses the same deficiencies shown above with respect to the Laudon, et al. and Yeager publications.

For the reasons set out above, the prior art cited by the Examiner fails to support the rejection of the claimed invention. Therefore, Applicant respectfully submits that

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Claims 1-20 are patentably distinct from the proposed Laudon,
et al. - Yeager - Agarwal - Goyette combination.

CONCLUSION


Applicant has clearly demonstrated that the present invention as claimed is clearly distinguishable over all the art cited of record, either alone or in combination, and satisfies all requirements under 35 U.S.C. §§101, 102, and 103, and 112. Therefore, Applicant respectfully requests the Board of Patent Appeals and Interferences to reverse the final rejection of the Examiner and instruct the Examiner to issue a Notice of Allowance of all claims.

The Commissioner is hereby authorized to charge any fees or credit any overpayments associated with this Application to Deposit Account No. 02-0384 of BAKER BOTTS L.L.P.

Respectfully submitted,

BAKER BOTTS L.L.P.

Attorneys for Applicant

A handwritten signature in dark ink, appearing to read "Charles S. Fish", is written over the printed name.

Charles S. Fish

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02 November 2009

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CLAIMS APPENDIX

1. (Previously Presented) A multi-processor system, comprising:

a plurality of processors, each processor including an integrated memory operable to provide/receive/store data, each processor including a central processing unit having an integrated memory controller operable to control access to the integrated memory and an integrated memory directory operable to maintain a plurality of memory references to data within the integrated memory and at least one memory reference to data within an integrated memory of a different processor;

an external switch coupled to each of the plurality of processors, the external switch operable to pass data to and from any of the plurality of processors, the external switch including an external directory, the external directory operable to provide a memory reference for each of the plurality of processors to remote data that is not provided within its own integrated memory directory.

2. (Original) The multi-processor of Claim 1, wherein the integrated memory directory is a cache buffer operable to hold a plurality of most recently accessed memory references.

3. (Original) The multi-processor system of Claim 2, wherein the integrated memory directory is operable to overwrite an oldest memory reference with a new memory reference upon reaching a buffer limit.

4. (Previously Presented) The multi-processor of Claim 1, wherein the integrated memory directory of a particular processor is operable to generate a directory request in response to not having a memory reference to data desired by its associated processor.

5. (Original) The multi-processor system of Claim 1, wherein the external directory is operable to receive a request for directory assistance from a particular one of the plurality of processors, the directory assistance request including a request for data not having a memory reference in the integrated memory directory of the particular one of the plurality of processors.

6. (Original) The multi-processor system of Claim 5, wherein the external directory is operable to generate a memory reference for the requested data.

7. (Original) The multi-processor device of Claim 5, wherein the external switch is operable to provide the generated memory reference to the integrated memory directory of the particular one of the plurality of processors in accordance with the request for data.

8. (Original) The multi-processor system of Claim 5, wherein the external switch is operable to provide the requested data to the particular one of the processors in response to the generated memory reference.

9. (Original) The multi-processor of Claim 1, wherein each of the plurality of processors includes an integrated network interface operable to communicate information to and from the external switch.

10. (Original) The multi-processor system of Claim 1, wherein the memory references in the external directory are represented in a same manner as memory references in a particular integrated memory directory.

11. (Previously Presented) A method of accessing data in a multi-processor system, comprising:

storing information in a local memory, the local memory being integrated within a particular one of a plurality of processors of the multi-processor system;

maintaining a list of memory references to the information in the local memory in a memory directory integrated with a central processing unit of the particular one of the plurality of processors;

maintaining at least one memory reference to information in the local memory of a different one of the plurality of processors in the memory directory integrated with the central processing unit of the particular one of the plurality of processors;

generating a request for data;

determining whether the data is associated with information stored in the local memory and has a memory reference in the memory directory;

forwarding the request to an external switch in response to the data not having a memory reference in the memory directory, wherein the data not having a memory reference to the local memory in the memory directory is stored in a remote memory;

identifying a memory reference for the data in response to the request;

obtaining the data from the remote memory via the external switch in response to the identified memory reference.

12. (Original) The method of Claim 11, further comprising:

obtaining the memory reference to the data stored in the remote memory.

13. (Original) The method of Claim 11, wherein the local memory is integrated with a particular one of a plurality of processors of the multi-processor system, the list of memory references being maintained in a memory directory integrated with the local memory in the particular one of the plurality of processors.

14. (Original) The method of Claim 13, wherein the identified memory reference is generated external to the particular one of the plurality of processors.

15. (Previously Presented) The method of Claim 13, further comprising:

obtaining the data in response to the memory directory maintaining a memory reference to the data.

16. (Previously Presented) A processor in a multi-processor system, comprising:

a local memory integrated in the processor and operable to provide/receive/store data;

a central processing unit;

a memory controller integrated in the central processing unit and operable to control access to and from the local memory;

a memory directory integrated in the central processing unit and operable to maintain memory references to data within the local memory, the memory directory operable to maintain at least one memory reference to data within a local memory integrated in a different processor, the memory directory operable to generate a data request for data not having a memory reference in the memory directory;

a network interface integrated in the processor and operable to provide the data request to an external directory external to the processor, the network interface operable to receive the data according to the data request.

17. (Original) The processor of Claim 16, wherein the memory directory maintains a list of most recently accessed memory references.

18. (Original) The processor of Claim 16, wherein the local memory has a capacity of four gigabytes of data and the memory directory has a capacity of eight megabytes of data memory reference.

19. (Original) The processor of Claim 16, wherein the network interface is operable to provide a memory reference generated by the external directory to the memory directory.

20. (Original) The processor of Claim 16, wherein the memory directory includes two to the power of eighteen memory references.

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EVIDENCE APPENDIX

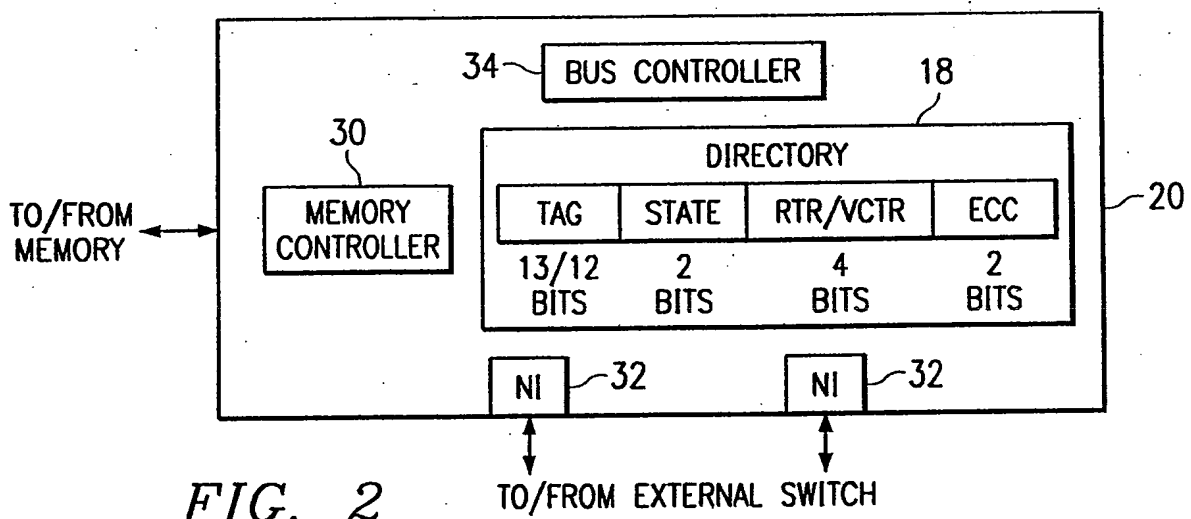
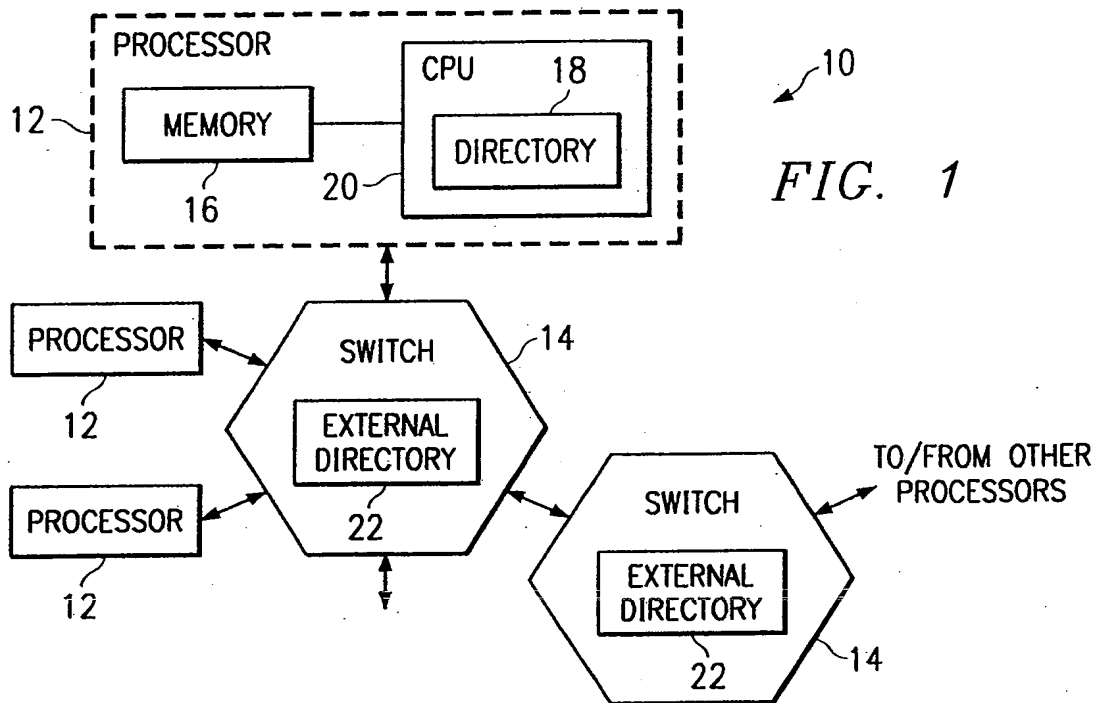
Attached herewith is a copy of page 2 from the Request for Continued Examination of May 23, 2006 showing changes to the specification to provide consistency with the drawing figures as requested by the Examiner.

Also attached herewith for reference purposes is a copy of a drawing sheet as originally filed showing FIGURES 1 and 2.

IN THE SPECIFICATION

Please replace the paragraph at page 8, line 24, beginning with "FIGURE 2 is a block diagram . . . " as follows:

FIGURE 2 is a block diagram ~~of a~~ of central processing unit 20 of processor 12. Central processing unit 20 of processor ~~Processor~~ 12 includes ~~memory 16,~~ a memory controller 30 to interface with memory 16, memory directory 18, one or more network interfaces 32, and a CPU controller 34. Network interfaces 32 provide a communication capability between processor 12 and external switch 22. Memory controller 30 controls the read and write access from and to memory 16. CPU controller 34 controls flow between one or more processing units.



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RELATED PROCEEDINGS APPENDIX

None

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CERTIFICATE OF SERVICE

None